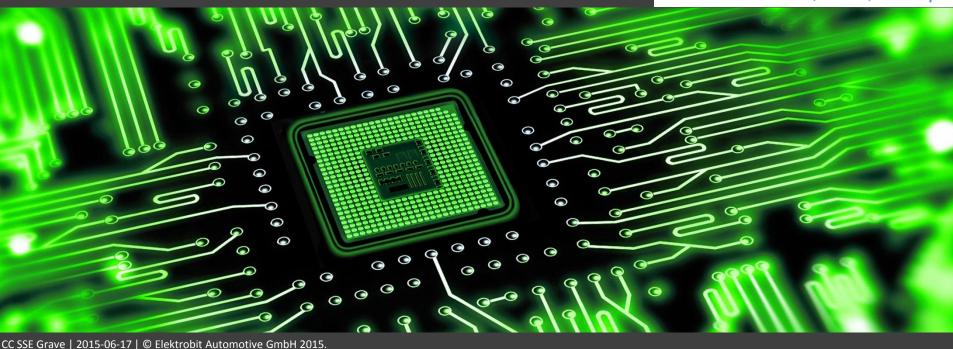
Software integration challenge multi-core – experience from real world projects





Rudolf Grave 17.06.2015



- About EB Automotive
- Motivation
- Constraints for mapping functions to cores
- AUTOSAR & MultiCore & Safety
- Summary & Outlook



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EB: Software and Services



Infotainment

Connected navigation software

- HMI tools for in-dash, digital instrument clusters and head-up displays
- Global software integration and engineering services

In-Car Infrastructure

- EB tresos integrated software and tools, based on AUTOSAR standards
- Solutions for: operating systems, middleware, dependable communication
- Solutions for high integrity systems: reliability, functional safety and security
- Test & simulation

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Driver Assistance

- Software development for driver assistance functions
- Electronic horizon and test drive recording solutions
- Driver assistance algorithms and functions

Connected

- Connected experiences around urbanization and electrification
- Online diagnostics
- Software and content updates

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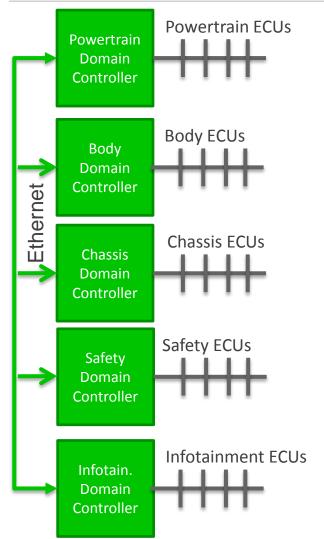
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Next generation of ECUs



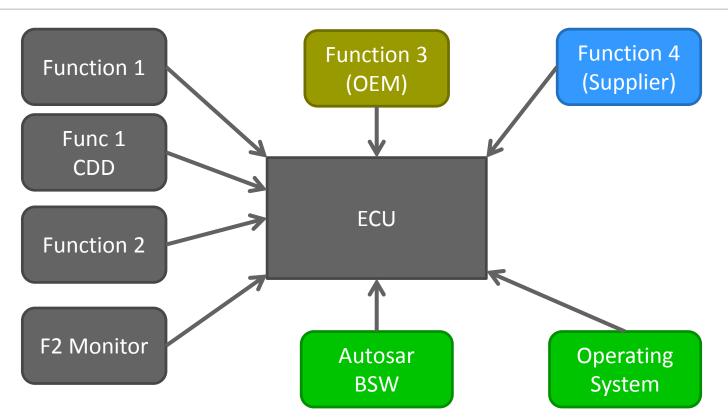
- Domain Controller will be huge multi-core systems
 - ECU independent function
 - Connected to Actuator / Sensor ECUs
 - Reloadable functions
 - Connected with Automotive Ethernet
- Domain ECUs will be "small" multi-core or single core systems
 - Hard real time
 - I/O handling
 - Safety functions
- Motivation for change current E/E architecture
 - Updatable ECUs
 - Dynamic Systems
 - Security

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AUT SAR

Motivation



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- "Welcome to the jungle!" (Herb Sutter)
- Automotive microcontroller follow IT systems with 5-8 years delay
- Appearing microcontroller
 - Different CPUs on one architecture
 - Combination of performance and peripheral cores

1975

- Combinations with DSP or GPUs
- Special microcontroller for special purpose

http://herbsutter.files.wordpress.com/2011/12/image thumb22.png?w=640&h=304

2005 2011

Welcome to the jungle

cloud-core

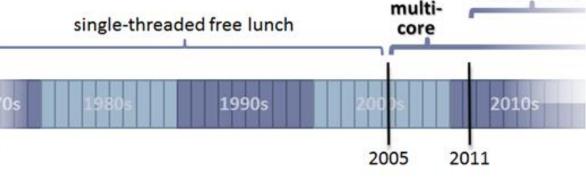
hetero-core

The free lunch is

so over



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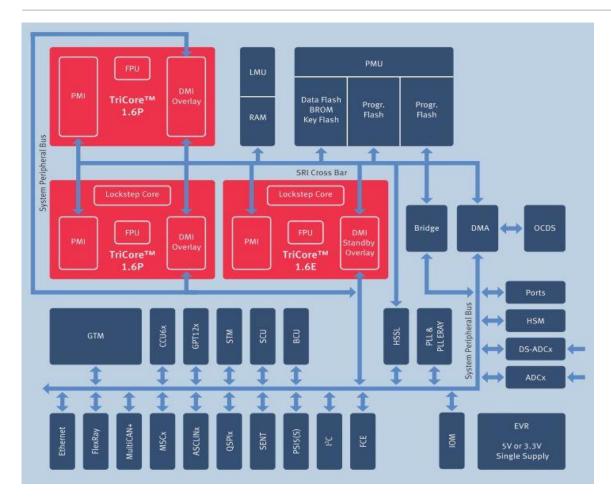




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Example: Infineon AURIX TC27x



Two lockstep cores

- 1.6E
- 1.6P

One non-lockstep core

• 1.6P

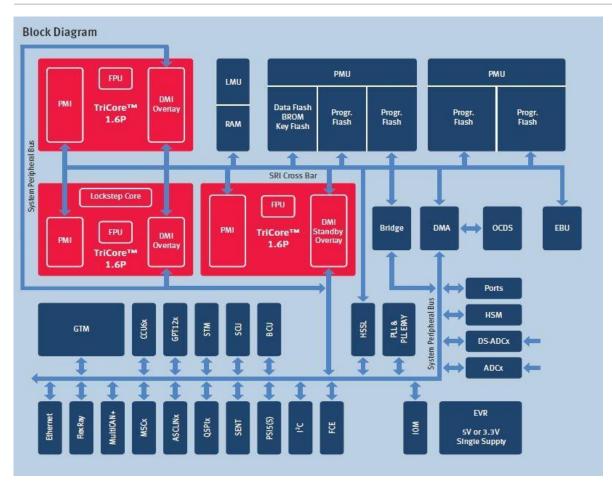
Source: http://www.infineon.com/export/sites/default/media/products/Microcontrollers/32bit/BlockDiagram-TC27xT.png



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Example: Infineon AURIX TC29x



One lockstep cores

• 1.6P

Two non-lockstep core

- 1.6P
- 1.6P

Source: http://www.infineon.com/export/sites/default/media/products/Microcontrollers/32bit/TC29xT_Block_Diagram.JPG

MPC5777M Block Diagram

Dec

imation

12x SAR

Example: Freescale MPC5777M

Computational Shell **Peripheral Control Shell** Debug 300 MHz Cores 200 MHz Core e200z7 in LS 200 MHz Crossbar 100 MHz Crossbar: 50 MHz Periphery **JTAG** e200z7 SWT e200z7 SWT e200z4 SWT 2x FlexRay Nexus 3+ STM STM STM Zipwire FPU FPU LFAST DSP INTC INTC INTC Ethernet Aurora VLE VLE FPU **eDMA** MCM MCM MCM Power Control 16 KB I-Cache 16 KB I-Cache VLE T Sensor Hardware 4 KB D-Cache I-RAM 16 KB 4 K D-Cache I-RAM 16 KB 8 KB I-Cache I-RAM 16 KB Security PMU Module Core MPU D-RAM 64 KB Core MPU Core MPU D-RAM 64 KB D-RAM 64 KB I-Fetch High-Bandwidth Crossbar Switch with ECC: 200 MHz Platform Crossbar Switch with ECC: 100 MHz System Memory Protection Unit System Memory Protection Unit Flash Control SRAM Control Bridge A Calib. Bus 16 KB External 404 K SRAM Periph. Periph. 8 MB 8 x 64 KB Overlay Buddy Device Bus (Includes 64 KB Flash EEPROM Interface RAM Interface Standby) SRAM 32 KB SRAM 54 KB

Source: http://cache.freescale.com/files/graphic/block_diagram/products/microcontrollers/AUT-P27692_MPC5777M_BDTN.jpg

6x LINFlex

8

dSPI

15x SENT

5×

PSI5

2×

PC

1x TT-CAN

8x PIT

4x M-CAN

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GTM104

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JTAGM

IMA

PASS TDM

Two computational core

- e200z7 (lockstep)
- e200z7

One peripheral core

e200z4

Bridge B

Periph.

14× CMU

MEMU

SIUL

STCU

Periph.

Dual PLL

FCCU

DTS

JDC

emapho

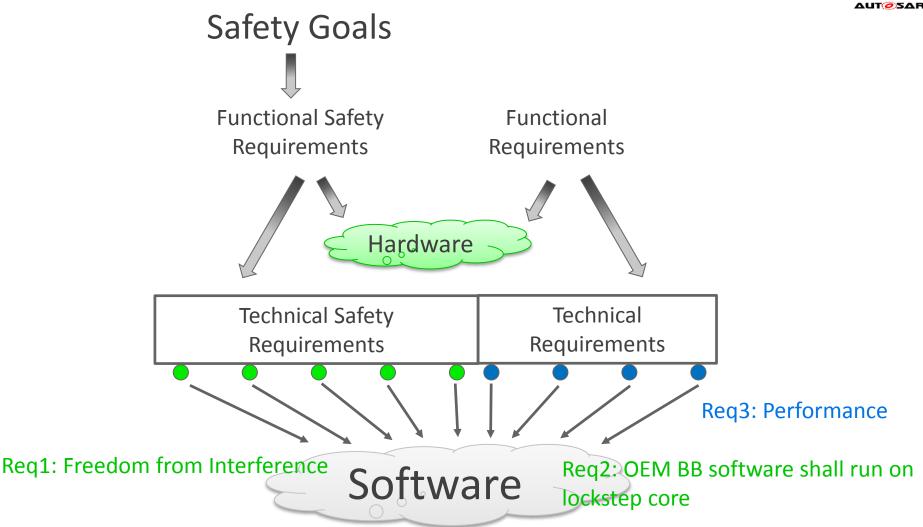
CRC







Constraint: Safety Goals



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Freedom from interference (ISO 26262)

In software partitioning system the freedom from interference argument between software component shall claim that:

- Shared resources are only used by one partition or a appropriate mechanisms are implemented
- Software partitioning is supported by hardware mechanism e.g. MPU
- Software mechanism ensuring FFI are implemented on highest level

Spatial FFI

"The data used by a one element shall not be changed by a another element. In particular, it shall not be changed by a non-safety related element."

Temporal FFI

"One element shall not cause another element to function incorrectly by taking too high a share of the available processor execution time, or by blocking execution of the other element by locking a shared resource"

Exchange of information

"Exchange of information shall be defined as transport of data between software elements or hardware. (e.g. messages between ECUs or cores, data from non-volatile memory)"

Software integration challenge multi-core

Functional Constraints

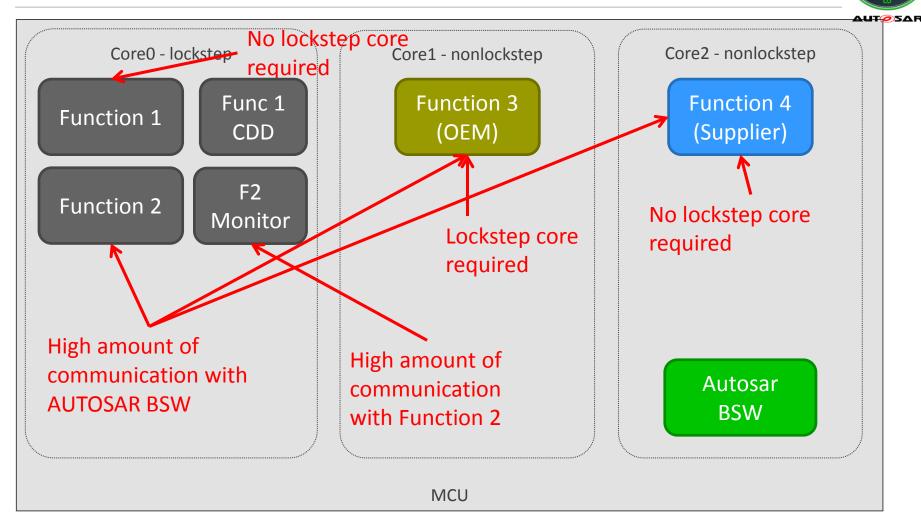
- AUTOSAR basic software < v. 4.0.3 can't be distributed on cores
- Reuse of legacy software
- Functional requirements
 - Response times
 - CPU load requirements
 - Startup times
 - Delay in Inter-Core, Inter-processor communication
- Access to peripherals





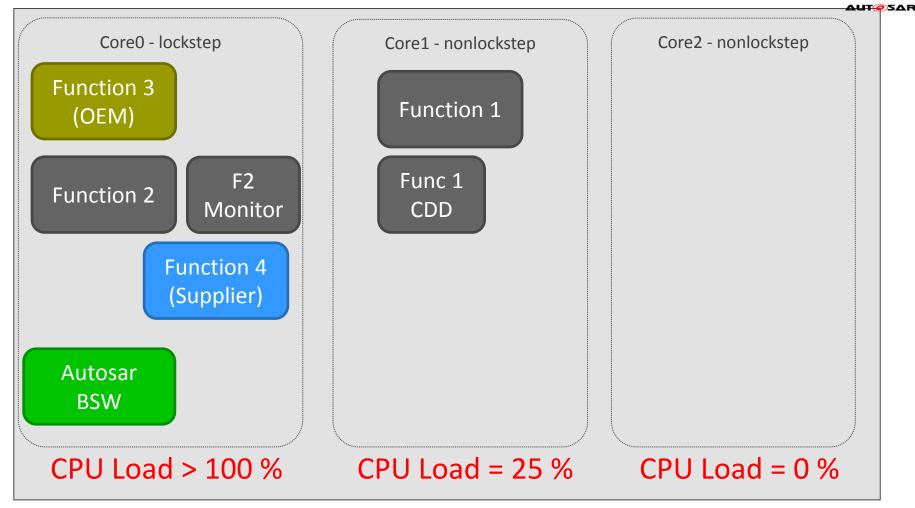


First idea: Group according to supplier



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Next idea



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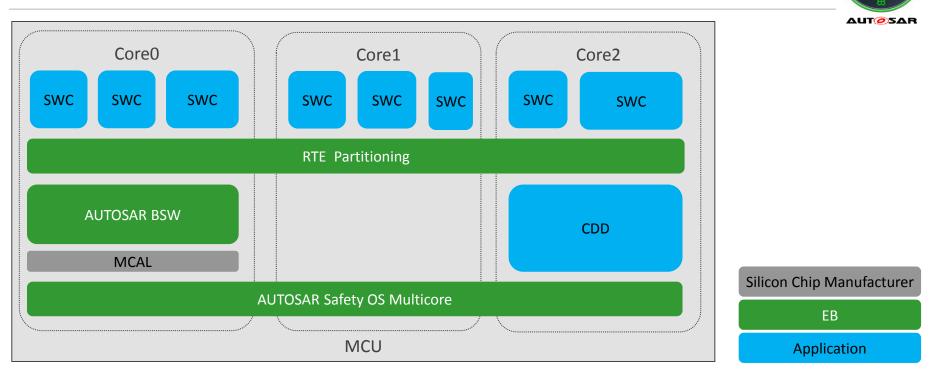
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AUTOSAR 4.0 – MultiCore



- AUTOSAR BSW runs on one core
- Safety OS MultiCore and Rte provides the ability to distribute AUTOSAR Software Components (SWC) to different cores

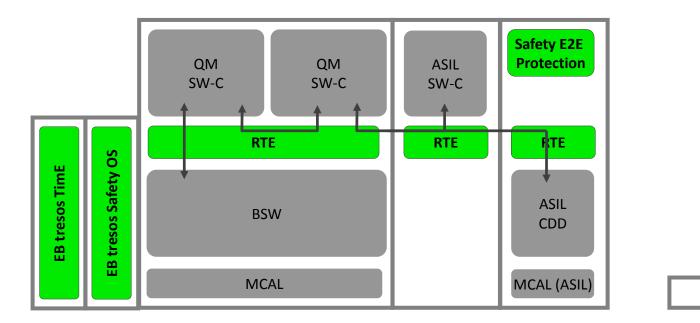
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Singlecore Safety architecture



Δυτ⊘sar



Partitions

EB tresos Safety products enable

- mix of QM and Safety Software (also different ASIL level)
- integration of Black-Box Software (independent from ASIL-Level)

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Os Applications

OS application

 Group of OS elements (ISRs, tasks, events, alarms,...)

Safety OS

• OS Applications are used to realize memory partition

MultiCore

- OS Applications are used for
 - Task to core mapping
 - ISR to core mapping

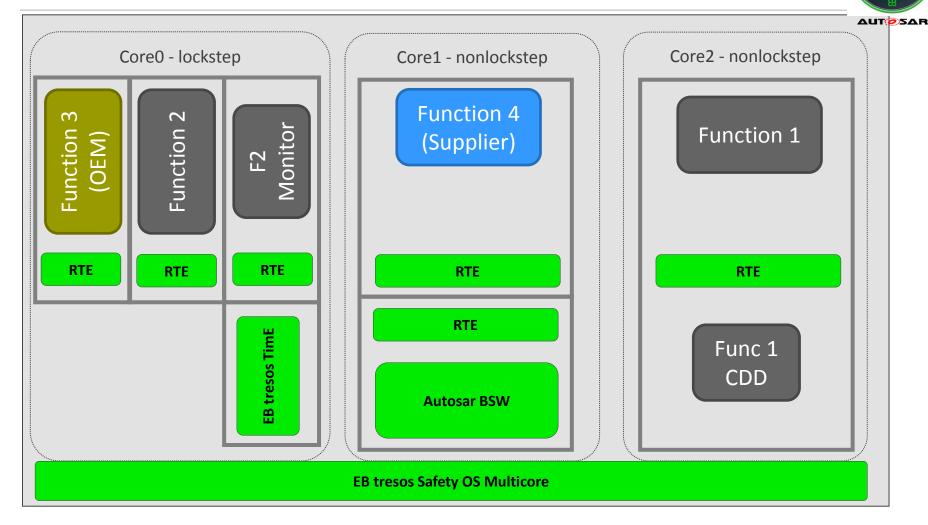


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OS App1 OS_App2 Data Data Task1 Task2 Task3 ISR1 Data Data Data Data Stack Stack Stack Stack **OS** Data Stack



Multicore Safety architecture



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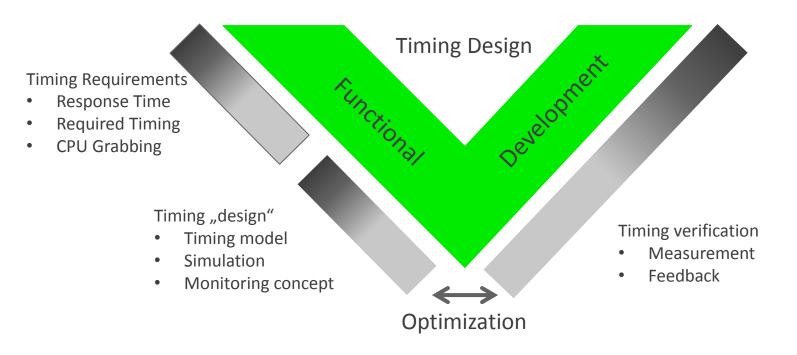








Summary: Software Architecture and early verification is the key to success

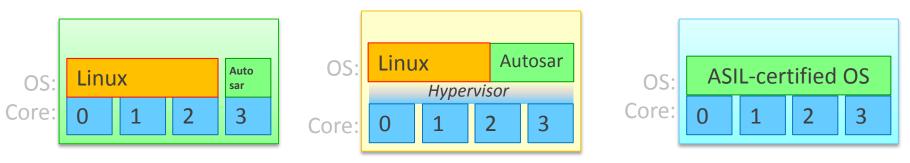


- Connect experts from functional development and infrastructure (Operating system and RTE)
- Functional expert can concentrate on algorithm
- Integration expert can concentrate on OS, RTE, Safety and performance



Outlook – "Reading the Crystal Ball"

- Multi-core systems are becoming a reality now and allow further consolidation of more functions on fewer ECUs
- Software system integration capabilities are key to success:
 - Taming the rising complexity
 - Building dependable, high-integrity systems
- Dynamic (service-oriented), dependable and high-integrity system architectures are required for future vehicles, e.g. autonomous driving.
 @EB you can evaluate / order such systems today (or soon) ^(C)
- Mixed operating system will come



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Contact us!



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